REMARKS

Claims 48-61 are pending the present application. Pursuant to an Office Action mailed July 11, 2001, claims 48-54 stand finally rejected.

The applicant thanks the Examiner for the courtesy of a telephonic interview held on October 2, 2001. As a follow-up to the interview, claims 55-61 have been added to further define the invention. Claims 55-61 relate to a method of forming a device for storing information as one of at least two possible stable current states. For the reasons offered below with respect to claims 48-54, claims 55-61 are believed to be in condition for immediate allowance.

Claim 48 stands rejected under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed intervention.

As used herein, the word "single" means "only one" and the drawings of the application show that each gate structure overlies only one junction. Therefore, claim 48 (as amended) is fully supported by the specification. Accordingly, the rejection of claim 48 under 35 USC § 112, first paragraph, is overcome.

Claims 48-50 and 52-54 stand rejected under 35 USC § 102(b) as being anticipated by United States patent number 5,346,838 issued to Ueno (Ueno). Reconsideration is requested.

The present invention relates to area efficient static memory cells employing parasitic bipolar transistors which can be latched in a bistable on state with small area transistors. Each bipolar transistor memory cell includes a gate which is pulse biased during a write operation to latch up the cell. Page 5, lines 7-13.

Ueno describes an insulated gate control thyristor whose current capacity is on the order of several tens of Amperes including a plurality of unit structures which are repeated in a lateral direction. Column 7, lines 24-27. According to Ueno, each gate is patterned by growing polysilicon film, or the like, over the entire surface of the wafer, and then by carrying out reactive ion etching using CCl_4 and Cl_2 on the polysilicon film to form patterns covering substantially the entire surface of each chip. Subsequently, a plurality of narrow stripe-like windows are formed in a direction normal to the sheet of figure 3 as shown in Ueno. Alternate first and second windows are formed in such a manner that each of the windows is a few micrometers to 10 micrometers wide, and adjacent windows are each spaced approximately the same distance apart. Each gate patterned on the base region serves as a mask for a p-type impurity implantation followed by annealing to form an emitter layer and a collector layer. Column 7, lines 38-54. Subsequently, an n-type cathode layer is formed in the emitter layer under a first window to a depth of about one

micron or less. Column 7, lines 62-64. The result, as is shown in figure 3, is a gate 20 overlying a plurality of junctions.

This is different from the structure claimed in claim 48, as amended, which claims forming at least one polysilicon gate overlying a single junction of a multi-region planar thyristor, thereby making the single junction a gated diode. The gate 20 of Ueno, as shown in figure 3, overlies a plurality of junctions, and thereby serves to form a MOS transistor 71, as illustrated in the schematic diagram shown in figure 4 of Ueno. Accordingly, the gate structure of Ueno, which covers a plurality of junctions, is different from the gate structure of the presently claimed invention which covers only a single junction, and results in the formation of a gated diode 26 as shown, for example, in figure 2 of the present application.

Claims 49-54 each depend directly or indirectly from claim 48, and incorporate every limitation thereof. Therefore, claims 49-54 are believed to be allowable over the prior art of record.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

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Version With Markings To Show Changes Made

48. (Twice Amended) A method of forming a circuit for storing information as one of at least two possible stable current states, the method comprising the following steps:

providing a semiconductor substrate;

providing doped silicon regions to form a multi-region planar thyristor having at least four regions;

forming at least one polysilicon gate overlying a [unique] single junction of said multi-region planar thyristor thereby making said [unique] single junction a gated diode; and

connecting said at least one polysilicon gate to a voltage source for producing latch-up in said multi-region planar thyristor.